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Power Electronics Education: A Contemporary Teaching Approach

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Abstract

Currently, there is a growing demand for methodologies that best qualify Engineering students at Universities. These methodologies require a substantial change in Engineering Teaching programs improving or even changing the traditional ways of imparting knowledge to students. In Power Electronics (PE) study the factors that make learning difficult for Electrical Engineering students, in order for them to achieve full understanding of the subjects addressed in a first discipline in this area, are the academic maturity required coupled with their multidisciplinary nature. The problem is aggravated in practical activities, which demand the availability of a laboratory infrastructure with specific characteristics not always available. An alternative for the study of PE, with a more contemporary focus, is to introduce, through a new Instructional Design (ID) Project, not only the incorporation of more hands-on activities that approach truly meaningful (authentic) contents. But also, new methodologies and technologies to support educational objectives that make full use of Digital Information and Communication Technologies (DICTs).This work proposes to develop and carry out a methodological design of a blended teaching for a Power-Electronics-based Practical Training Program (PEBPTP) for students of the Electrical Engineering Course of the Universidade

Federal do Maranhão in Brazil. The proposed program is mainly based on the use of a digital controller (unified) based on FPGA, developed and realized specifically for control and power inverters study. From controller's VHDL Code already realized, a Reuse Logic Block is generated (Intellectual Property Core (IP Core)), for use within the LabVIEW FPGA Hardware Description Environment. A Graphical Interface (GUI), more intuitive, and developed from the LabVIEW environment, will support the realization of the PEBPTP, for parameterizing the Controller, and show relevant figures of merit of the performance of the converter being study. The active methodologies, converging with the diverse possibilities of resources of the DICTs, implanted in the classroom, with the adequate contextualization of the specific resources of each area, contribute increasingly to the student being protagonist of their own knowledge construction. Finally is proposed, and in full adherence to a novel trend, that both the PEBPTP and the unified controller previously developed in FPGA are embedded in what is being named Lab-on-a-Chip (LoC). This embedded structure will allow access to the laboratory hands-on program via a web service that uses a fully Programmable Logic Device (PLD) that incorporates an integrated structure known as System-on-a-Chip (SoC). The above proposals and experiences involve the mastery not only of curricular and technological knowledge, inherent to the training of an Engineer, but of mainly, the pedagogical technological knowledge and correct use of DICTs. At this point, in particular, is founded our contribution within the context of Engineering Teaching, to advance in the improvement or perhaps in the modification of the "classroom" of Engineering courses, which today go beyond the physical space of the University.

Keywords: Active Methodologies, Blended Teaching, DICTs, Instructional Design, PEBPTP.

1. Introduction

Currently, there is a growing demand for methodologies that best qualify Engineering students at Universities. These methodologies require a substantial change in Engineering Teaching programs improving or even changing the traditional ways of imparting knowledge to students[1]. Particularly, to obtain the required advancements in the study and in contemporary power electronic (PE) applications will be only possible with the student engaged with a solid and active education in this area[2,3].

An alternative, with a more contemporary focus, is to introduce, through a new ID Project, not only the incorporation of more hands-on activities that approach truly meaningful (authentic) contents, but also, new methodologies and technologies to support educational objectives that make full use of DICTs[4].

It is consensus that the so-called Active Methodologies (AM), which are teaching methods that enable the student to participate actively in the classroom, contributing and having more autonomy about his learning process, is particularly important in maintaining the dynamism of the teaching-learning process. Since the flow of content depends not only on a previous script done by the teacher, but also on the student's activity.

In PE Study the factors that make learning difficult for Electrical Engineering students, in order for them to achieve full understanding of the subjects addressed in a first discipline in this area, are the academic maturity required coupled with their multidisciplinary nature. The problem is aggravated in practical activities, which demand the availability of a laboratory infrastructure with specific characteristics not always available[5,6].

Accelerated technological advances in the area impose greater rigor in the availability of didactic resources, though both from the points of view of content and form, since they must facilitates the construction of knowledge, mediates the interaction between student and teacher, and develop specific skills and competences. In practical activities, the demands for Authentic Learning experiences are an increasingly necessity within the classroom. Accor-

ding to Brown, J.S (1989): *"Authentic learning situates students in learning contexts where they encounter activities that involve problems and investigations reflective of those they are likely to face in their real world professional contexts"*[7].

On the other hand, as stated in Quezada (2018)[4], to make effective the methodological reformulation of a certain subject of study is not a trivial task for teachers of the areas of Sciences and Technology, particularly with respect to Engineering Education. The process demands the need to appropriate academic and methodological techniques in the areas of teaching and pedagogy. In addition, Mishra and Koehler (2006)[8] argue that just introducing technology into the teaching-learning process is not enough. For the authors, today, teachers will always have to update knowledge about the use of DICTs and incorporate them into their practices. Technological knowledge has become an important category of knowledge related to teaching.

This work proposes to develop and carry out a methodological process to construct a blended teaching program for a Power-Electronics-based Practical Training Program (PEBPTP), for a first discipline in PE, applying ID techniques and Active Methodologies, focusing the study and experimentation in Voltage Source Inverters. Are outlined all the important aspects take into account to construct the referred program.

Power Inverters are power static converters that transform electrical power from continuous to alternating power sources (DC/AC Converters). These have a wide industrial application, both in isolated systems, as in the case of Electronically Controlled Machine Drives widely used in industry, or in Grid-tie Systems, such as in distributed generation systems that use alternative energy sources (Smart Grids). Voltage Source Inverters (VSI) is the most common power converters in power electronics, after rectifiers[9].

The PEBPTP is based on the use of a digital controller (unified) based on FPGA[10], developed and realized for control and power inverters study. The designed FPGA controller allows the selection and parameterization of different architectures of single-phase and three-phase DC-AC converters as well as the selection of different operating modes, from square wave to PWM, so that the student of Electrical Engineering can study and assimilate difficult concepts in a mild and iterative way. In this work, from the controller already performed, a Reuse Logic Block is generated (Intellectual Property Core (IP Core)), for use within the LabVIEW FPGA Hardware Description Environment. Developed from the LabVIEW FPGA, for parameterizing and show relevant figures of merit of the performance of the particular inverter architecture selected for study, a Graphical Interface (GUI), more intuitive, will support the PEBPTP.

Finally, and in full adherence to a novel trend[1,11,12], it is proposed that both the PEBPTP-VSI and the unified controller previously developed in FPGA are embedded in what is being named Lab-on-a-Chip (LoC). This embedded structure will allow access to the laboratory hands-on program via a web service that uses a fully programmable logic device (PLD) that incorporates an integrated structure known as System-on-a-Chip (SoC).

2. The Instructional Design Process

One of the greatest challenges faced by most teaching professionals in the fields of technology and the exact sciences is the search for an efficient learning method due to the enormous number of different models, methods and techniques. Issues arise immediately after a teacher proposes to adopt such methodologies in the classroom, especially in Engineering Education. How to proceed effectively to adopt, incorporate and operationalize these methodologies in the classroom? What are the pedagogical knowledge needs and methodologies, and not acquired by the teacher during his/her Engineering qualification?

In executing an ID project, not only curricular, pedagogical and technological pedagogical aspects must be taken into account, but also, legal remedies imposed by the Ministry of Education. Particularly in Brazil, for the teaching of Engineering, the Curricular Guidelines.

The ID is an area focused on Educational Research, where is made study of techniques, methods and resources to support the teaching-learning process[13]. Using ID, we can build a new methodological solution that effectively improves teaching quality in any teaching program. The ID Matrix (IDM), the result of this instructional reformulation, is one of the fundamental tools for proposing and managing the contents approached through the application of the new methodology.

Related to this proposal, and as in Quezada (2018)[4], the authors made use of the ADDIE method to develop the ID Project of the proposed teaching program.

The ADDIE method is composed of five phases: *analysis, design, development, implementation* and *evaluation*. In what follows, we will describe this method applied to the ID Project of PEBPTP-VSI.

2.1. ADDIE Method - PEBPTP-VSI Analysis

In the process of instructional design carried out, the first step (*analysis*) is where we define the objectives of the course, gather information about the purpose of the instructional project and observe the variables that will be useful for the development of our solution.

The instructional aspects analyzed in this stage were:

- Learning needs;
- The characteristics of the target audience; and
- Lifting of restrictions.

The learning needs refer to the general and specific objectives of the course, the skills that students need to acquire. Is also identified the learning environment and the technologies that to be used during the course.

The target audience of the discipline is undergraduate students of the Electrical Engineering Course formally enrolled in the discipline of PE of UFMA.

In the aspect of lifting of restrictions, we defined the prerequisites to participate in the discipline, how the content will be passed to the students, the technical limitations and the resources.

Power Electronics comprises: *connection, disconnection, control* and *transformation of electric power*, using for this *static power converters* composed of *semiconductor power devices*. As well as *command, control* and *regulation circuits*.

At the Universidade Federal do Maranhão/Brazil, the subject of the practical discipline of PE, deals with:

- Projects, simulations and practices;
- Applications of power semiconductors: diodes and thyristors; and
- Operation of basic converters: rectifiers and inverters.

In order to support practical activities, within a contemporary perspective, the Laboratory of Models, Objects and Prototypes of Learning to Support the Teaching of Power Electronics and Electronic Instrumentation (LabMOPA-EPI). Has proposed, within its guidelines of produce didactical support material and methodologies to support the teaching

of Electrical Engineering, the development of several PEBPTPs focusing on the study of Static Power Converters that performs the Basic Static Conversion Functions of AC-DC and DC-AC.

Particularly, for the PEBPTP-VSI, the methodological approach scope to VSIs study was defined as[9,14,15]:

1. Single Phase Topologies:
   - Half Bridge:
     - Square Wave Mode of Operation; and
     - PWM Mode (Carrier-Comparison).
   - Full Bridge:
     - Square Wave Mode of Operation; and
     - PWM Mode (Carrier-Comparison):
       - Bipolar; and
       - Unipolar.
2. Three Phase Topologies:
   - Square Wave Mode of Operation:
     - 120°; and
     - 180°.
   - PWM Mode:
     - Sinusoidal PWM (SPWM); and
     - Third Harmonic Injection PWM (THIPWM).

From the defined scope, in the next step were formulated content units and hands-on activities executed within the context of the program.

2.2. ADDIE Method - PEBPTP-VSI Design

The second step of the ADDIE (*design*) method is where we plan content units; define their objectives and instructional strategies to achieve them[16]. It is the phase where we define the rules that will ensure that each laboratory practice runs systematically.

The planning starts from the definition of content units and objectives of each laboratory practice, through the definition of the roles that each individual will play in the teaching-learning process as well as the tools and resources used by the students.

In planning the PE laboratory discipline, the following variables had to be carefully planned:

- Basic content units;
- Learning goals to be achieved;
- Roles of the different actors involved;
- Practical and meaningful activities;

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- Expected duration for each unit of content;
- Content to be addressed in each unit;
- Technological support tools; and
- Evaluation process.

At the end of this phase, we collected enough information to generate the Instructional Design Matrix (IDM). The IDM is a fundamental tool in the management of the educational process, providing us with a table of all the steps and information we need to implement for each basic unit of defined content.

Of particular importance, later, when specifying the LoC, is the definition of Laboratory Functions.

Within the current context, Laboratory Functions refers to the development of theoretical and practical skills and competences through the development of significant experimentation practices within the field of Electrical Engineering.

Within this context, Laboratory Functions refer:

a) Collect, acquisition, organization, processing, presentation, measuring and analysis of experimental information; and

b) Access, parameterization and control of the experimentation base in current use.

The basic VSI study of the PEBPTP-VSI considered the following experimental aspects and answered the questions:

1. The conversion process: Products and By-products. What products and by-products are these?
2. The operational behavior of the conversion system: From the point of view of the power electronic switches that constitute the inverter and with a view to defining operating limits. What are the power electronic switches? What operational limits are these?
3. Effects of the by-products of the conversion process: on the load and on the source of entry: What products and by-products are these? What effects do the by-products produce on the load and the input source?
4. Basic VSI inverter control techniques: Frequency, Voltage, others.

The experiments planned as pilots to the proposed methodology were:

a) Laboratory 1: Introduction to Control of Voltage Source Inverter – Operating Principle of the FPGA (Unified) Digital Controller.

Objective: Students will have access to and understand the basic operating principles behind the FPGA (Unified) Digital Controller design, which supports PTPBEP-VSI.

In this practice, the student is initially literate in the use, resources and technical characteristics of the FPGA (Unified) Digital Controller.

The goals are:

- That the student known about the fundamentals of the VSI Control;
- Introduce to the Square Wave VSI Mode Control;
- Introduce to the Pulse Width Modulation VSI Mode Control;
- Present the student the FPGA (Unified) Digital Controller specifically developed to support the PEBPTP-VSI; and

- Introduce and literate the student in the use, resources and technical characteristics of the FPGA (Unified) Digital Controller.

The proposed carried out practices are:

- *Exercise 1-1*: Simulation, using MULTISIM, of a basic Square Wave Digital Controller;
- *Exercise 1-2*: Simulation, using MULTISIM, of a basic PWM Digital Controller;
- *Exercise 1-3*: Understanding the basic functional blocks of the FPGA (Unified) Digital Controller and its operating modes. Internal signal generation fundamental, parametrization and control resources, trigger signals generation and steering circuits; and
- *Exercise 1-4*: Using the FPGA (Unified) Digital Controller for PEBPTP-VSI.

b) Laboratory 2: Single Phase Voltage Source Inverters – Square Wave Mode Control.

Objective: Conduct the student through practical and meaningful experience in the basic principle of VSI operation using a single-phase bridge architecture operating in square wave mode.

In this practice, the student learn the physical operation of a VSI, verifying the basic products and by-products of the static inversion process.

The goals are:

- That the student verify and understand in practice about the basic power inversion principle;
- That the student verify and recognize in practice the products and by-products resulting of the static inversion process;
- That the student make a graphical analysis and measurements, using the LabVIEW resources, of the figures of merit resulting of the static inversion process;
- That the student understand and verify in practice the relationship between: (a) DC Voltage Source of the Inverter; (b) Inverter architecture and controls; (c) Products and by-products resulting of the static inversion process; and
- Inverter architecture and controls; (c) Products and by-products resulting of the static inversion process.

The proposed carried out practices are:

- *Exercise 2-1*: Understanding the basic inversion principle – Operation of the single-phase bridge VSI in square wave mode: (a) With R Load; (b) With R-L Load. Products and by-products;
- *Exercise 2-2*: Graphically Analyzing and measuring of figures of merit of the single phase-bridge inverter operating with: (a) R Load, and; (b) R-L Load; and
- *Exercise 2-3*: Verifying in practice the relationship between: (a) DC Voltage Source of the Inverter; (b) Inverter architecture and controls; (c) Products and by-products resulting of the static inversion process.

c) Laboratory 3: Three Phase Voltage Source Inverters – Square Wave Mode Control.

OBJECTIVE: Conduct the student through practical and meaningful experience in the basic principle of VSI operation using a three-phase bridge architecture operating in Square Wave Mode. In this practice, the student will study a practical architecture of a VSI, verifying the operation in 120° and 180° modes.

The goals are:

- That the student verify and understand in practice about the basic power inversion principle using a three-phase bridge architecture;
- That the student verify and recognize in practice the products and by-products resulting of the static inversion process and the difference and advantages of this three architecture when compared to the single-phase one;
- That the student make a graphical analysis and measurements, using the LabVIEW resources, of the figures of merit resulting of the three-phase static inversion process; and
- That the student understand and verify in practice the relationship between: (a) DC Voltage Source of the Inverter; (b) Inverter architecture and controls; (c) Products and by-products resulting of the static inversion process.

The proposed carried out practices are:

- *Exercise 3-1*: Understanding the basic three-phase inversion principle – Operation of the three-phase bridge VSI in square wave 120o mode: (a) With R Load; (b) With R-L Load. Products and by-products;
- *Exercise 3-2*: Graphically Analyzing and measuring of figures of merit of the three-phase bridge inverter 120o operating with: (a) R Load, and; (b) R-L Load;
- *Exercise 3-3*: Verifying in practice the relationship between: (a) DC Voltage Source of the Inverter; (b) Inverter architecture and controls; (c) Products and by-products resulting of the static three-phase inversion process 120o;
- *Exercise 3-4*: Understanding the basic three-phase inversion principle – Operation of the three-phase bridge VSI in square wave 180o mode: (a) With R Load; (b) With R-L Load. Products and by-products;
- *Exercise 3-5*: Graphically Analyzing and measuring of figures of merit of the three-phase bridge inverter 180o operating with: (a) R Load, and; (b) R-L Load; and
- *Exercise 3-6*: Verifying in practice the relationship between: (a) DC Voltage Source of the Inverter; (b) Inverter architecture and controls; (c) Products and by-products resulting of the static three-phase inversion process 180o.

d) Laboratory 4: Three Phase Voltage Source Inverters – Sine PWM Mode Control.

Objective: Conduct the student through practical and meaningful experience in the basic principle of operating the VSIs using a three-phase bridge architecture, operating in Sinusoidal PWM mode.

In this practice, the student will study a practical architecture of a VSI, verifying the operation in Sine PWM mode.

The goals are:

- That the student verify and understand in practice about the basic power inversion principle using a three-phase bridge architecture operating in Sine PWM;
- That the student verify and recognize in practice the products and by-products resulting of the static inversion process and the difference and advantages of this three architecture, in SPWM Mode Control, when compared to the three-phase one, in square wave mode control;
- That the student make a graphical analysis and measurements, using the LabVIEW resources, of the figures of merit resulting of the three-phase static inversion process in Sine PWM;
- That the student understand and verify in practice the relationship between: (a) DC Voltage Source of the Inverter; (b) Inverter architecture and controls; (c) Products and by-products resulting of the static inversion process; and
- Inverter architecture and controls; (c) Products and by-products resulting of the static three-phase inversion process in Sine PWM Mode Control.

The proposed carried out practices are:

- *Exercise 4-1*: Understanding the basic three-phase inversion principle – Operation of the three-phase bridge VSI in Sine PWM mode: (a) With R Load; (b) With R-L Load. Products and by-products;
- *Exercise 4-2*: Graphically Analyzing and measuring of figures of merit of the three-phase bridge inverter operating with: (a) R Load, and; (b) R-L Load; and
- *Exercise 4-3*: VVerifying in practice the relationship between: (a) DC Voltage Source of the Inverter; (b) Inverter architecture and controls; (c) Products and by-products resulting of the static three-phase inversion process in Sine PWM Mode Control.

e) Laboratory 5: Three Phase Voltage Source Inverters – THIRD HARMONIC INJECTION PWM (THIPWM) Mode Control.

Objective: Conduct the student through a meaningful and practical experimentation of VSIs using a three-phase bridge architecture, operating in THIPWM mode.

In this practice, the student will study a practical architecture of a VSI, verifying the operation in Sine PWM mode.

The goals are:

- That the student verify and understand in practice about the basic power inversion principle using a three-phase bridge architecture operating in THIPWM;
- That the student verify and recognize in practice the products and by-products resulting of the static inversion process and the difference and advantages of this three architecture, in THIPWM Mode Control, when compared to the three-phase one, in square wave mode control;
- That the student make a graphical analysis and measurements, using the LabVIEW resources, of the figures of merit resulting of the three-phase static inversion process in THIPWM; and

- That the student understand and verify in practice the relationship between: (a) DC Voltage Source of the Inverter; (b) Inverter architecture and controls; (c) Products and by-products resulting of the static inversion process.

The proposed carried out practices are:

- *Exercise 4-1*: Understanding the basic three-phase inversion principle – Operation of the three-phase bridge VSI in THIPWM mode: (a) With R Load; (b) With R-L Load. Products and by-products;
- *Exercise 4-2*:Graphically Analyzing and measuring of figures of merit of the three-phase bridge inverter operating with: (a) R Load, and; (b) R-L Load; and
- *Exercise 4-3*: Verifying in practice the relationship between: (a) DC Voltage Source of the Inverter; (b) Inverter architecture and controls; (c) Products and by-products resulting of the static three-phase inversion process in THIPWM Mode Control.

2.3. ADDIE Method - PEBPTP-VSI Development

As discussed earlier, in this work are discussed and used educational methodologies and models and, for the Engineering project, the work discusses and uses technological methodologies and tools to develop the hardware's support platform for the training program.

After the planning stage, we started the third step of the ADDIE model, developing all the contents and resources planned in the IDM, was also necessary to elaborate all didactic materials, activities and the evaluations process.

2.3.1. Blended Learning

As mentioned previously, in Brazil, and by virtue of the Curricular Guidelines imposed by the Ministry of Education, for the teaching of Engineering, the possibility of expanding the distance methodologies for undergraduate courses in the area of Engineering is only possible for 20 % of its workload. In this sense, and in order to comply with this legal restriction imposed, in the proposal of the PEBPTP-VSI is inserted in the Blended teaching methodology.

According to Mill, Daniel (2018): *"Blended Learning is characterized by the use of combined or mixed solutions, involving the interaction between the modalities of presence and non-presential teaching, the interaction between pedagogical approaches and the interaction between technological resources*[17]*"*.

As mentioned earlier, Mishra and Koehler (2006)[8] argue that just introducing technology into the teaching-learning process is not enough. For the authors, today, educators will always have to update knowledge about the use of DICTs and incorporate them into their practices. Technological knowledge has become an important category of knowledge related to teaching.

We are at a stage of technological development where online presence through the Internet, and through today's technological communication devices, can be as (or more) communicative and engaging as the physical presence in the conventional classroom.

A known AM for integrating presential and non-presential moments, that reverses the moments of acquisition and application of knowledge, is the *Flipped Classroom*. In this work, this is the adopted methodology to grant to the program the Blended character proposed. In the context of the program, the Blended approach is proposed as a means to:

- Promote space-time flexibility to the way the contents would be accessed/studied;
- Provide access to the proposed contents in a ubiquitous way;
- Teach the contents and promote their complementation through the use of On-Line research tools;
- Promote the accomplishment of activities with tools of productivity in group;
- Open a virtual space for collaborative work groups and collaborative discussion; and
- Access the web service of LoC working ambient, related to PEBPTP-VSI.

2.3.2. Active Methodologies: Flipped Classroom Strategy

Traditional learning methods have as characteristic the transmission of information from the teacher to the student. The active learning methods, however, put the student in the focus of the teaching-learning process, giving him a more active role within the classroom, creating opportunities for the development and construction of knowledge[18].

AM, by exploiting work in teams, generally contribute to the improvement of interpersonal relationships and cooperative work[19], making the student research, reflect and decide what to do to achieve the established learning goals, promoting his motivation[20].The Flipped Classroom (FC) active learning method is the strategy used in this work to enable an active learning for students in PE discipline.

The FC methodology has as basic principle the fact that the student has prior access to the subject material that will be studied, leaving the face-to-face meeting with the teacher in the classroom for deeper discussions about the content doubts that will arise. In traditional teaching models, the teacher normally transmits information in its entirety in the classroom, the student's function is to absorb information and try to construct knowledge by solving problems and developing projects after school, but not all students can assimilate past information and have a good performance.

In this work, the learning objectives to be achieved in the new instructional reformulation were established taking into account the hierarchy of cognitive levels of the learning process proposed by the Bloom Taxonomy, which deals with the abilities of knowledge, understanding and intellectual development[21]. Figure 1 shows the six cognitive levels as originally proposed by the Bloom Taxonomy.

Bloom Taxonomy is one of the existing tools that facilitate the structuring process of the ID, and its main purpose is to assist in the planning, organization and control of learning objectives[22].

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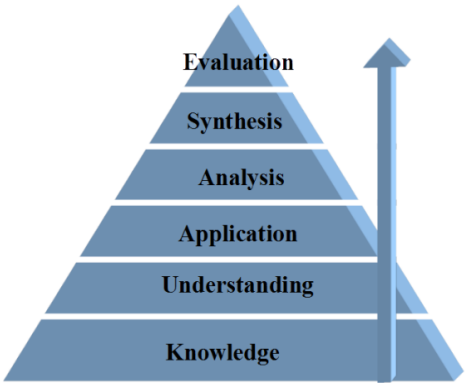

Figure 1. The six cognitive levels of Bloom's taxonomy.

To fit the execution of the activities planned for each laboratory, with the hierarchical levels defined by Bloom, each of them is divided into three moments, choosing the FC methodology as a way to enhance students' Authentic Learning:

- Before-Class Stage: Covers the remembering and understanding cognitive levels of the Bloom Taxonomy. At this stage, the student should remember and understand the content that is passed to him;

- In-Class Stage: Classroom moment, held in the laboratory. Before starting the hands-on experimentation, the student perform an online test where the Before-Class stage studies will be ascertained. From this test will be verified in which of the topics covered the students had greater difficulty, thus allowing the teacher to generate debates to clarify the doubts. At this point, it is possible to verify the inversion of the classroom, since it is no longer the teacher who will conduct the discussion by exposing the subject to the students, but the students who will rescue the content studied in the previous stage and have a more active participation in class, discussing the subject and doubts. The Classroom moment covers the cognitive levels of application and analysis of the Bloom Taxonomy, uses the concepts learned previously to solve the tasks and analyze the proposed problems; and

- After-Class Stage: Step held after the time in the classroom. At this stage, the student will receive a task as a challenge on the subject addressed in the classroom stage. A forum is open in the LMS where the teacher should use to answer questions about the proposed task. The After-Class stage covers the cognitive levels synthesis and evaluation of the Bloom Taxonomy, where the student combines the knowledge acquired in previous steps to create their own applications.

The Figure 2 shows how the three proposed learning moments in the Bloom Taxonomy and when the classroom inversion occurs.

In each of the three Moments of the learning process, the student evaluation is fulfilled. In the Before-Class and After-Class Moments, is carried out outside the classroom, with the support of the LMS. In the case of the classroom stage, the student's presence, participation in the debates, involvement in the conduct of practical activities and presentation of the results count for assessment purposes.

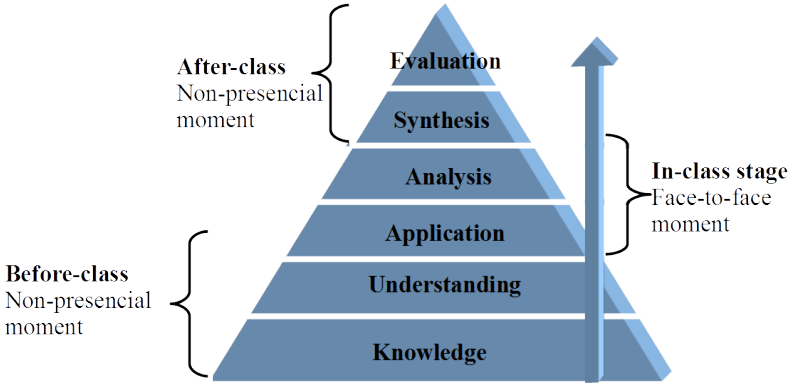

Figure 2. The six levels of the Bloom taxonomyand the three adopted learning moments.

Prior to laboratories 1, 2, 3, 4 and 5, is programmed a Laboratory 0. This is an exclusively face-to-face moment at the beginning of the activities of the practical course, where students are introduced to the new methodology to be adopted, the objectives, the roles of each one, routines to be performed (activities), the contents and resources to be used. It is also explained the systematic evaluation of each stage or moment.

2.3.3. Virtual Learning Environment

In this stage, was planned the Virtual Learning Environment (VLE). It is through the VLE that there will be interaction between Engineering educators and students while outside the classroom, making effective the Flipped Classroom methodology. Therefore, it is imperative that the LMS offer the right tools for this purpose.

Into the activities proposed, the technological support resources were thought as a means of:

- Constitution of a Virtual Room of the program through an LMS, to post activities and content, making spatial and temporal access flexible;
- Access to learning materials in the form of videos and tutorials, webinars, etc.;
- Creation of discussion forums to post doubts/ propositions/socialization of research materials, among others;
- Content management;
- Creation of questionnaires;
- Online chat system; and
- System for monitoring students' progress.

In the Virtual Learning Environment of the Power Electronics program, for each experimental practice, the three learning moments were implemented (Before-Class, In-Class and After-Class). MOODLE was the LMS of our choice.

2.3.4. Unified FPGA Digital Controller

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With the student's engagement, the development and realization of PEBPTP-VSI's support platform began with the a revision of a unified FPGA-based Digital Controller10, designed to operate according to the architectures and modes of operation of the VSI defined previously, in the analysis step (ADDIE).

2.3.4.1. Controller Original Design

The controller can be schematized as the combination of three main blocks shown in Figure 3. The diagram shows the basic elements of the FPGA controller (a), together with VSI Topologies Studied and Operating Modes proposed (b).

The Unified Digital Controller was developed through the PLD Design tool or PLD Schematic, an integral part of the NI-MULTISIM Spice Capture and Simulation tool (Student Edition)[23].

The digital controller was projected and accomplished to be capable of generating trigger signals in nine different operating modes10, which differ from one another in:

a) Number of phases and architecture of the power inversion studied; and

b) Control technique used to generate the trigger signals of the specific power inverter selected.

In Table I are listed the nine operating modes of the controller, related to a specific identification number (ID). In addition, the respective power switches driven by the controller for each ID selected. Figure 4 shows the power inverter's IGBTs architecture used in the project.

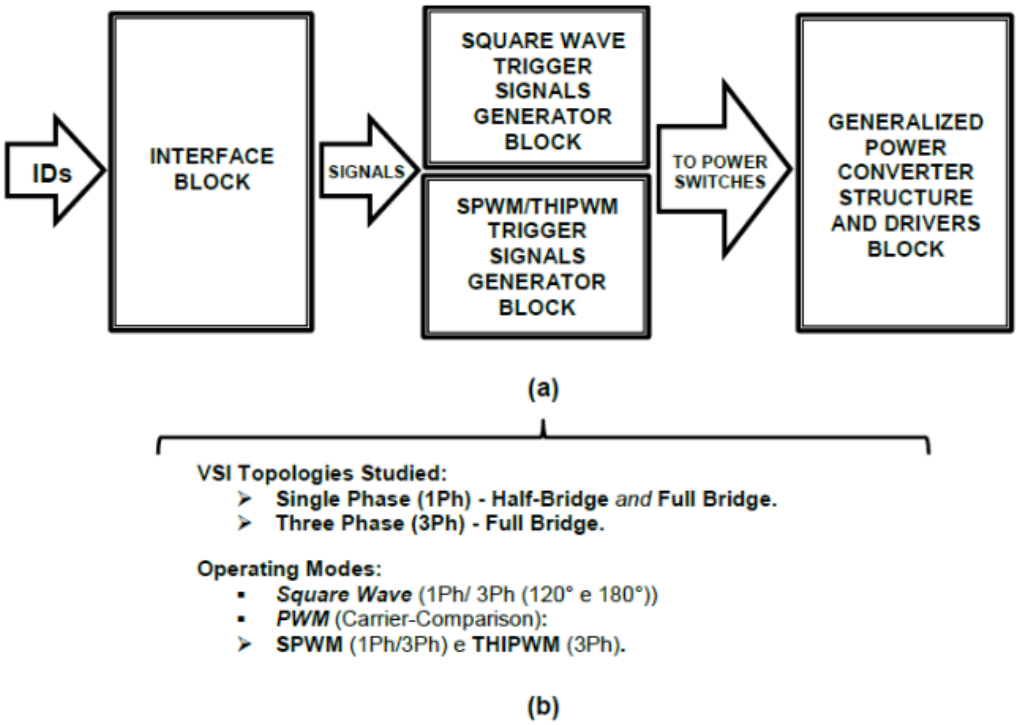

Figure 3. Unified FPGA Controller Designed for VSI Inverter Study - PLD-Design Project Cycle. (a) General Block Diagram Basic Elements. (b) Topologies Studied and Operating Modes proposed.

Table 1. Operating modes of the FPGA controller.

ID	Phases	Power Switches	Topology	Control Technique
1	1-Ph	SwA_U, SwA_L	Half Bridge	Square Wave
2	1-Ph	SwA_U, SwA_L SwB_U, SwB_L	Full Bridge	Square Wave
3	3-Ph	SwA_U, SwA_L SwB_U, SwB_L SwC_U, SwC_L	Full Bridge	Square Wave 120°
4	3-Ph	SwA_U, SwA_L SwB_U, SwB_L SwC_U, SwC_L	Full Bridge	Square Wave 180°
5	3-Ph	SwA_U, SwA_L SwB_U, SwB_L SwC_U, SwC_L	Half Bridge	SPWM
6	1-Ph	SwA_U, SwA_L SwB_U, SwB_L	Full Bridge	SPWM Bipolar
7	1-Ph	SwA_U, SwA_L SwB_U, SwB_L	Full Bridge	SPWM Unipolar
8	3-Ph	SwA_U, SwA_L SwB_U, SwB_L SwC_U, SwC_L	Full Bridge	SPWM
9	3-Ph	SwA_U, SwA_L SwB_U, SwB_L SwC_U, SwC_L	Full Bridge	THIPWM

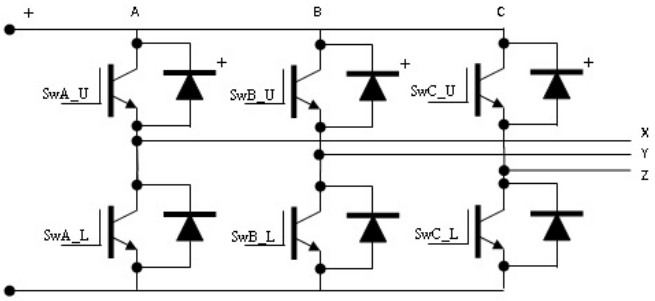

Figure 4. IGBT's Power Inverter Architecture used.

2.3.4.2. PLD Design Environment

As already mentioned, this project was carried out originally using the PLD Design or PLD Schematic Co-simulation tool[23], an integral part of the NI-MULTISIM (Student Edition) Spice capture and simulation tool, which shows students the system-based design cycle in FPGA, but making reference and use of the discrete logic that they learn in the basic discipline of Digital Circuits.

PLD design tool in conjunction with Xilinx's ISE design tools, which make use of VHDL (VHSIC Hardware Description Language), allows the construction of a (program) logical structure and results in a description file of logic behavior for synthesis of the hardware to be written into an FPGA. This tool shortens the cycle of FPGA-based projects, since

it partly exempts the learning and mastery of a HDL, since the systems being designed refer directly to the projects in discrete logic, using as basic components families of Low-Scale-Integration Logic Blocks widely used in basic courses of digital circuits (e.g. TTL, CD).

2.3.4.3. NI-DEFB/XILINX Development Platform

In this work, we use the Digital Electronics FPGA Board (DEFB) Development Platform, which integrates a FPGA from Xilinx. Developed for use with the Experimentation and Data Acquisition Platform NI-ELVIS II. The DEFB features a Xilinx XC3S500E Spartan-3E FPGA[24]. In addition to the FPGA, the Platform contains other development support components. The DEFB Platform is a Development Targets supported by PLD Design Tool.

2.3.4.4. The Graphical System Design LabVIEW Platform

Due to the inherent graphical limitations of PLD-Design development environment, there are no simple means to obtain the visualization of the internal signals of the controller or any other resource that would aid in the study of power inverters, making it difficult to use it as a teaching tool.

In this way, it is essential to make use of a development environment that provides the necessary laboratory function resources to create a graphical and interactive interface that allows the use of the functions and signals related to the inverter architecture studied and Controller that, as previously mentioned, we refer to these as the laboratory functions.

The LabVIEW[25] environment is system-Engineering software designed specifically for applications that require testing, measurement, and control that also has tools for building more interactive and user-friendly graphical interfaces, offering an approach that allows the visualization of each aspect of the inverter architecture, the controller and its respective signals generated.

LabVIEW FPGA[26] module is an add-on module for Lab VIEW. Using the LabVIEW FPGA Module, it is possible develop custom control and measurement hardware without any prior knowledge of hardware description languages or board level hardware design. This add-on module also provides the reuse of VHDL codes in the form of IP Cores, to build future applications more quickly. When using NI LabVIEW FPGA to develop applications for FPGA deployment, you need to follow some additional guidelines for building code modules (subVIs) that take advantage of FPGA-specific behavior. This way, the LabVIEW platform features greater advantage of use to expand the resources of the unified FPGA-based Digital Controller in order to make it, in fact, an educational platform to support Engineering Education.

2.3.4.5. Intellectual Property Core (IP Core)

The technological solution for use the unified FPGA-based Digital Controller in the LabVIEW FPGA development module involves exporting the controller's VHDL code from PLD-Design/Multisim environment and generate an IP Core block to reuse into the LabVIEW FPGA development environment.

An IP Core, for definition, is a logical unit, cells or reusable circuit layout projects used in Application-Specific Integrated Circuit (ASIC) or FPGA prototypes[27,28].

Thus, from the unified FPGA-based Digital Controller, we sought to create the IP Core for transferring this controller for implementation and synthesis of the graphical interfaces

in LabVIEW.

The LabVIEW FPGA Hardware Description Environment (HDL) provides two methods for third-party IP Core reuse:

- Component-Level Intellectual Property (CLIP); and
- IP Integration Node.

The basic difference between the two is that the CLIP node runs independently and in parallel with the application developed in LabVIEW FPGA, while the IP Integration Node is inserted in the block diagram of the LabVIEW FPGA, running in the manner defined by the data stream of the VI. Thus, the IP Integration Node tool is more suitable for the developed controller.

2.3.4.6. IP Integration Node

To create the IP Integration Node of the Unified Controller, we exported the file in MULTISIM/PLD Design to VHDL code, by means of the transfer option present in the toolbar of the PLD Design generating two files, responsible for the definition of the components (Top-level architecture) and their connections, respectively. In Figure 5, it is shown the block diagram of the export process of the VHDL code to the creation of IP Core.

In the next steps, the code syntax is checked and the support files, clock definition and synchronous and asynchronous ports, and process termination generated, resulting in a component with Boolean inputs and outputs, as shown in Tables 2 and 3.

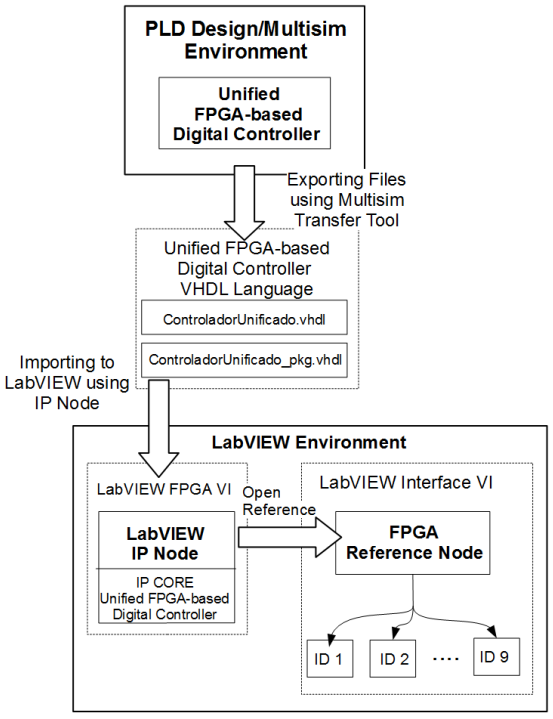

Figure 5. VHDL code export process block diagram to the core IP creation.

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Table 2. LabVIEW Integration Node Architecture - Input Pins.

Input Pins
Select
Increment
Decrement
Reset
On/Off
Phase Sequence Control
RotCLK

Table 3. LabVIEW Integration Node Architecture - Output Pins.

Output Pins
SwA_U Driver/LED1
SwA_L Driver/LED0
SwB_U Driver /LED3
SwB_L Driver /LED2
SwC_U Driver/LED5
SwC_L Driver/LED4
ID's Visualization Signals (7 Segments Display)
Intermediate Signal - 8 bits Triangular Carrier
Intermediate Signal - 8 bits Phase A Sine Reference
Intermediate Signal - 8 bits Phase A Sine Reference
Intermediate Signal - 8 bits Phase A Sine Reference with THI

All the input pins of the IP Node preserve their respective function, as projected in the original development, as indicated in Table 4. Table 5 indicates the Driver Signal to the Power Devices, where LED0, LED1, LED2, LED 3 and LED5 are the DEFB's LEDs.

Table 4. Controller Integration Node Block Selection/parameterization inputs.

IP Node Input Pins Function	Description
Select	Selects the controller's operating mode (ID) and starts the operation process. Enables the trigger signals at the controller output and disables the mode identifier increment/decrement buttons
Increment	Increments the operating mode identifier, if in selection process (ID → 01 ... 09).
Decrement	Decrements the operating mode identifier, if in selection process (ID → 09 ... 01).
Reset	Places the controller in the starting point. Returning to the selection process, that is, it disables the outputs of the Controller and enables the increment and decrement buttons of the mode identifier.
On/Off	On/off. Enables or disables the controller, blocking the outputs if in the off position. The SW0 slide switch must be kept off to ensure that no spurious firing signals are generated after the FPGA programming process or in the process of energizing the Platform, serving as protection to the power inverter being controlled.
Phase Sequence	Changes the phase sequence (ABC↔ CBA). It changes the counting direction (Up↔ Down) of the counters present in the signal generation blocks, thus changing the phase sequence at the inverter output. It only works in three-phase modes.
RotClk	Reference frequency input pin. Controller's frequency adjust of the output frequency of the power inverter.

Table 5. Controller Integration Node Block Driver Signals Outputs.

IP Node Output Control Pins	Description
SwA_U Driver/LED1	Controller's output driver signal directed to Power Device SwA_U
SwA_L Driver/LED0	Controller's output driver signal directed to Power Device SwA_L
SwB_U Driver /LED3	Controller's output driver signal directed to Power Device SwB_U
SwB_L Driver /LED2	Controller's output driver signal directed to Power Device SwB_L
SwC_U Driver/LED5	Controller's output driver signal directed to Power Device SwC_U
SwC_L Driver/LED4	Controller's output driver signal directed to Power Device SwC_L

2.3.4.7. Graphical User Interface (GUI)

The GUI is the way through which the PEBPTP-VSI will become an interactive and user-friendly experience for students that apply to the VSI training program. The GUI's project must include:

a) Elements to parameterize and control the operation of the unified FPGA-based Digital Controller. In this way, the GUI must incorporate:

- Graphical elements to implement the controls appointed in Table II. Furthermore, must incorporate necessary graphical elements to identify the ID setting in current use; and
- Graphical elements to control and identify Controller's operating parameters, like frequency, phase sequence operation adjust, and so on, related with the settled ID.

b) Incorporate support to all the Laboratory Functions previously described. Exploring with advantage the experimental measurement and signal processing capabilities of the LabVIEW environment. Specifically, must support:

- Visualization of important Controller's internal signals, which is defined by the ID setting;
- Visualization of important Inverter's experimental figures of merit, like ac and dc voltages and currents, from the current architecture and mode operation, which is defined by the ID setting; and
- Visualization of Inverter's signal processing of important figures of merit, like spectra, THD, vector diagrams, from the current architecture and mode operation, which is defined by the ID.

c) Be perfectly adherent with the training program proposed.

In this way, the LabVIEW GUI project must take into account all the aspects indicated above.

2.4. ADDIE Method - PEBPTP-VSI Implementation

2.4.1. Instructional Design Result (IDM)

We present in Table 6, as an example, the resulting ID Matrix (IDM) for the content unit defined as Laboratory 1. This IDM is the result of the instructional reformulation realized through this work, and is one of the fundamental tools for proposing and managing the contents approached through the application of the new methodology. As we can observe, in this Matrix are inserted the all methods and pedagogical methodologies previously discussed:

- ADIEE Method;
- Blended Learning;
- Flipped Classroom Strategy; and
- Bloom Taxonomy.

From the ID Matrix, was planned the VLE. As was mentioned earlier, MOODLE was the LMS of our choice. For the purpose of construction of the VLE, the ID Matrix is the tool of fundamental importance. Note that the ID Matrix already consider the three learning moments were implemented: *Before- Class, In-Class* and *After-Class.*

Laboratory of Digital Models, Prototypes and Learning Objects to Support the Teaching of Power Electronic and Electronic Instrumentation - LabMOPA-EPI

ID MATRIX - DISCIPLINE PLAN

DISCIPLINE: POWER ELECTRONICS LABORATORY.
ACADEMIC RESPONSIBILITY AND INSTRUCTIONAL DESIGNER: PROF JOSÉ ROBERTO QUEZADA PENA (jrkezada@yahoo.com).
INSTRUCTIONAL DESIGN ASSISTANTS: BRENDA IRLA CARDOSO (brenda_irla@hotmail.com) AND JEFFERSON WILLIAM CUNHA DE OLIVEIRA (williamoliveira183@hotmail.com).
SCHOOL SEMESTER: 2019-2 DATE: 17/04/2019 VERSION: APRIL 2019

CONTENT UNIT	GOALS	ROLES	ACTIVITIES	DURATION	CONTENT	TOOLS	EVALUATION
Lab 1 – Introduction to Control of Voltage Source Inverter – Operating Principle of the FPGA (Unified) Digital Controller.	i. That the student known about the fundamentals of the VSI Control; ii. Introduce to the Square Wave VSI Mode Control; iii. Introduce to the Pulse Width Modulation VSI Mode Control; iv. Present the student the FPGA (Unified) Digital Controller specifically developed to support the PEBFTP-VSI; v. Introduce and iterate the student in the use, resources and technical characteristics of the FPGA (Unified) Digital Controller.	**Students:** ✓ Reading and understanding of the indicated references; ✓ Register doubts to lead through On-Line tutoring or in the classroom session.	**Before-Class Stage** In sequence, Posted in Virtual Learning Environment: • Read the Paper "Teaching Digital Logic Fundamentals - Theory, Simulation and Deployment." • Study the content presented in the Tutorial "FPGA (Unified) Digital Controller." • Study the Tutorial "Introduction to the NI-ELVIS Workstation as DAQ Device." • Read the "Digital Electronics FPGA Board User Manual." **In-Class Stage** • To Apply "On-Line" test to verify the use of before-class studies, and extract individualized reports indicating the gaps detected and skills developed. • To promote a debate adjusted to the results informed by the "On-Line" test report, in order to overcome the identified gaps and consolidate the skills developed. • Run the Lab Exercise Guides: i. Exercise 1-1: Simulation, using MULTISIM, of a basic Square Wave Digital Controller; ii. Exercise 1-2: Simulation, using MULTISIM, of a basic PWM Digital Controller; iii. Exercise 1-3: Understanding the basic functional blocks of the FPGA (Unified) Digital Controller and its operating modes. Internal signal generation fundamental, parameterizations and control resources, trigger signals generation and steering circuits; iv. Exercise 1-4: Using the FPGA (Unified) Digital Controller for PEBFTP-VSI. • Formulate *"Challenge"* for After-Class Stage. **After-Class Stage**	3 Class/Hours 4 Class/Hours 3 Class/Hours	○ Paper. *"Teaching Digital Logic Fundamentals - Theory, Simulation and Deployment."* ○ Tutorial *"FPGA (Unified) Digital Controller."* ○ Tutorial *"Introduction to the NI-ELVIS Workstation as DAQ Device"*. ○ User Manual. *"Digital Electronics FPGA."* ○ "Quizes." ○ "On-Line" Test and "On-Line" test report. ○ Lab Exercise Guides. ○ After-Class *"Challenge"*.	○ Virtual Learning Environment. ○ NI ELVIS II Benchtop. ○ LabVIEW and MULTISIM Softwares and Add-Ons. ○ DEFB and PEBFTP-VSI's support platform. ○ Laboratory Assistant and Trainee support. ○ Web and IT support.	Before-Class Stage: ○ Effective participation and total accomplishment of the proposed activities; ○ Total accomplishment of *"Quizes"* relative to Webinar and Tutorials. In-Class Stage: ○ Presence in the classroom; ○ Involvement and active participation of the activities of debate and formulation of difficulties or doubts; ○ Involvement in the performance of practical activities and presentation of results. After-Class Stage: ○ Effective participation and performance of proposed activities; ○ Presentation of the results proposed in the *"Challenge"*.

Students:
✓ Track, summarize and understand additional reference content;
✓ Perform *"Challenge"*;
✓ Cure on-line doubts about the challenge.
Professor:
➢ Clarify doubts;
➢ Suggests additional support material, if necessary.

• On the scheduled date, port, in the Virtual Learning Environment of the discipline, the result of the *"Challenge"* formulated in the classroom.

Table 6. Instructional Design Matrix of Laboratory 1.

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2.4.2. Virtual Learning Environment (MOODLE)

Quezada, et. al. (2018) reported[4]: *"MOODLE is a platform that offers a wide variety of interactive administrative and pedagogical tools, both synchronous and asynchronous, facilitating the educator's work in the construction and availability of materials and execution of learning and follow-up activities".*

Its choice is due to the facility of operationalize the proposed methodology due to the many resources and tools that the platform offers, as shown in Figure 7[4].

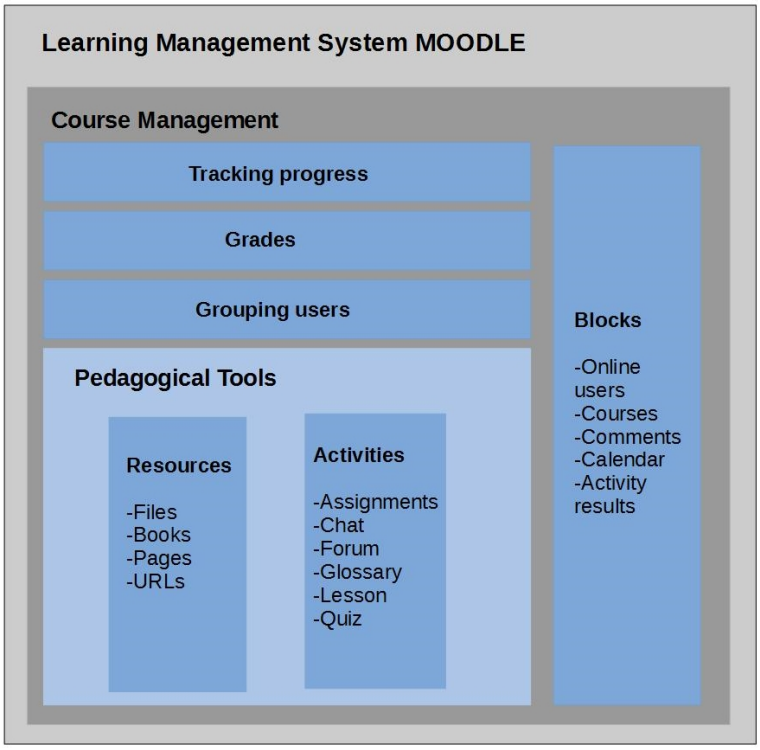

Figure 7. Resources used in the construction of the Virtual Learning Environment.

2.4.2.1. Graphical User Interface (GUI)

In that follow, we present practical results. Figure 8 shows the GUI planned and implemented for controller parameterization. Pay attention at controls and indicators planned for Controller's control.

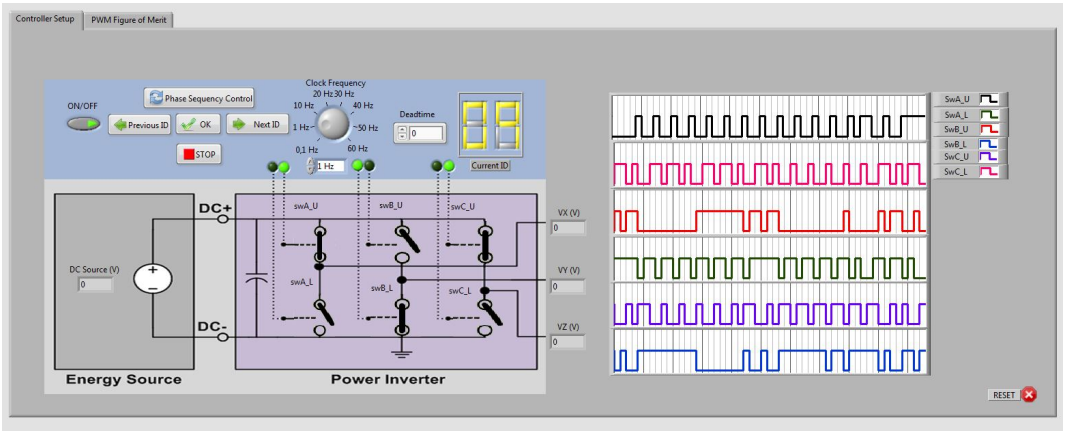

Figure 8. GUI Screen for ID = 09 with controller parameterization and control.

In Figure 9 shows GUI results for Controller's internal signals of merit, for PWM operation.

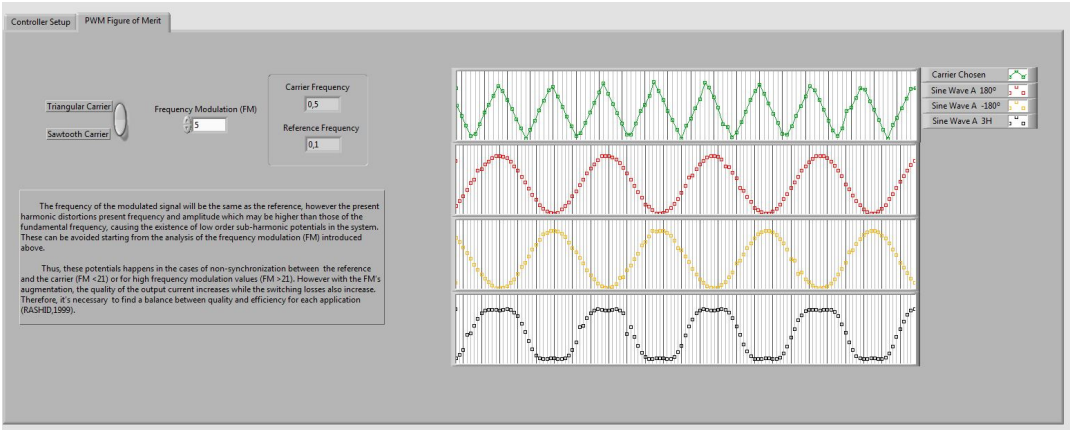

Figure 9. GUI Screen PWM operation with controller's internal signals of merit.

According to Table 7, the IDs of 02, 03 and 04 are shown in Figures 10, 11 and 12, respectively.

Table 7. Operating modes of the FPGA controller – Examples of practical GUI results.

ID	Phases	Power Switches	Topology	Control Technique	GUI Screen
02	1-Ph	SwA_U, SwA_L SwB_U, SwB_L	Full Bridge	Square Wave	Figure 10
03	3-Ph	SwA_U, SwA_L SwB_U, SwB_L SwC_U, SwC_L	Full Bridge	Square Wave 120°	Figure 11
04	3-Ph	SwA_U, SwA_L SwB_U, SwB_L SwC_U, SwC_L	Full Bridge	Square Wave 180°	Figure 12

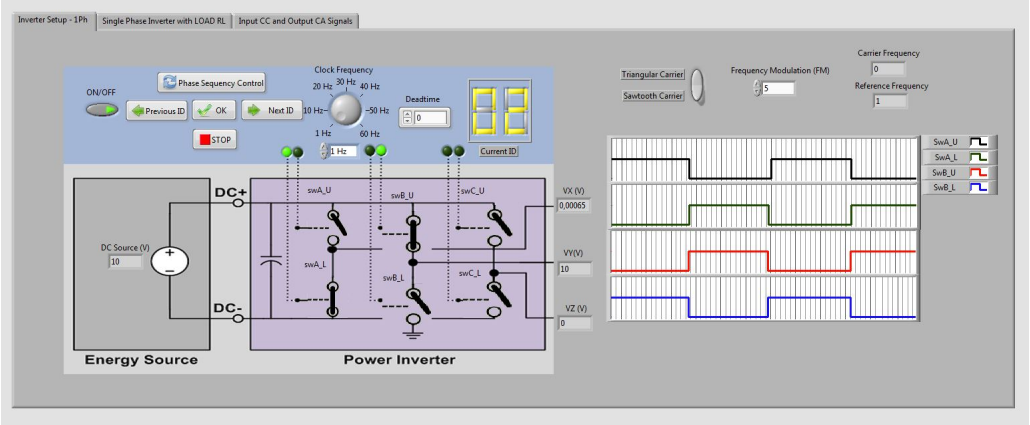

Figure 10. GUI Screen for ID = 02 with single phase full bridge VSI, square wave mode of operation.

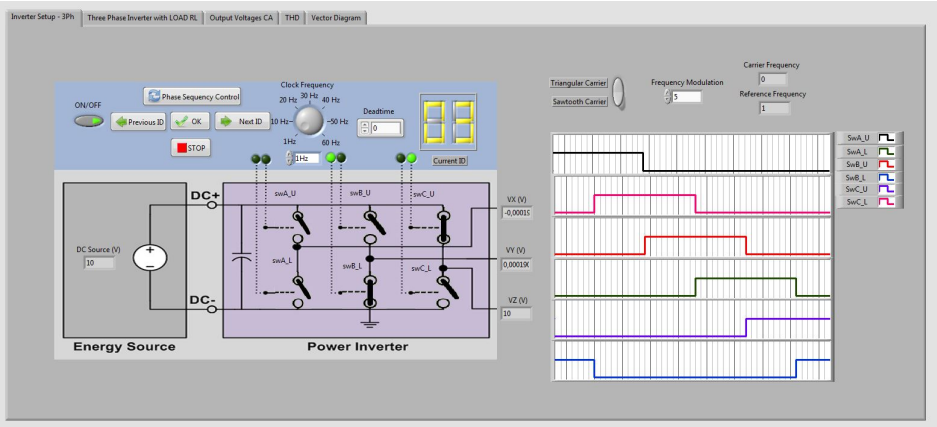

Figure 11. GUI Screen for ID = 03 with three phase full bridge VSI, square wave mode of operation 120°.

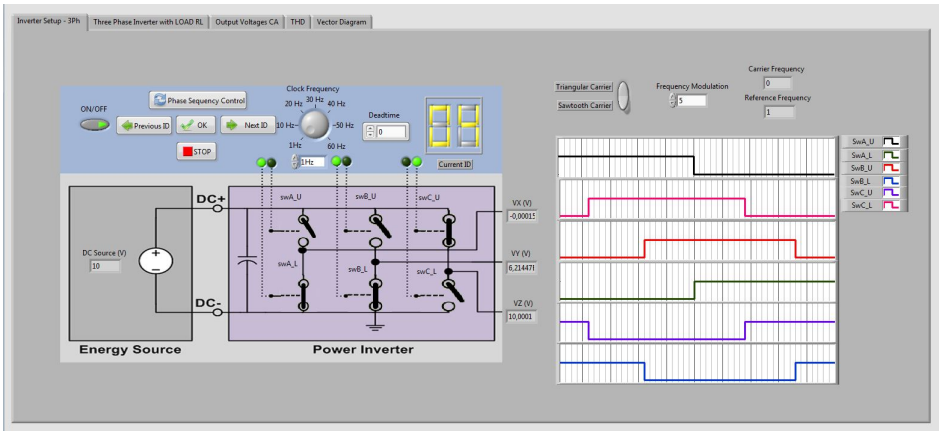

Figure 12. GUI Screen for ID = 04 with three phase full bridge VSI, square wave mode of operation 180°.

According to Table 8, the IDs of 08 and 09 are shown in Figures 13 and 14, respectively.

Table 8. Operating modes of the FPGA controller – Examples of practical GUI results.

ID	Phases	Power Switches	Topology	Control Technique	GUI Screen
08	3-Ph	SwA_U, SwA_L SwB_U, SwB_L SwC_U, SwC_L	Full Bridge	SPWM	Figure 13
09	3-Ph	SwA_U, SwA_L SwB_U, SwB_L SwC_U, SwC_L	Full Bridge	THIPWM 120°	Figure 14

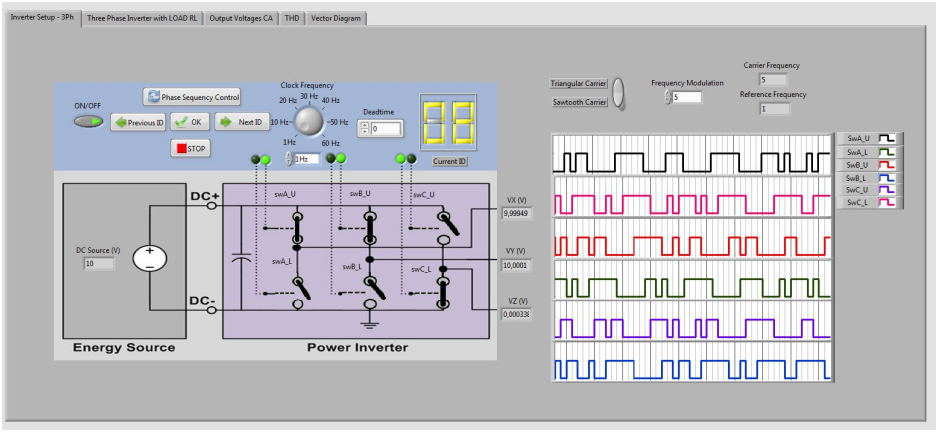

Figure 13. GUI Screen for ID = 08 with three phase full bridge VSI, SPWM mode of operation.

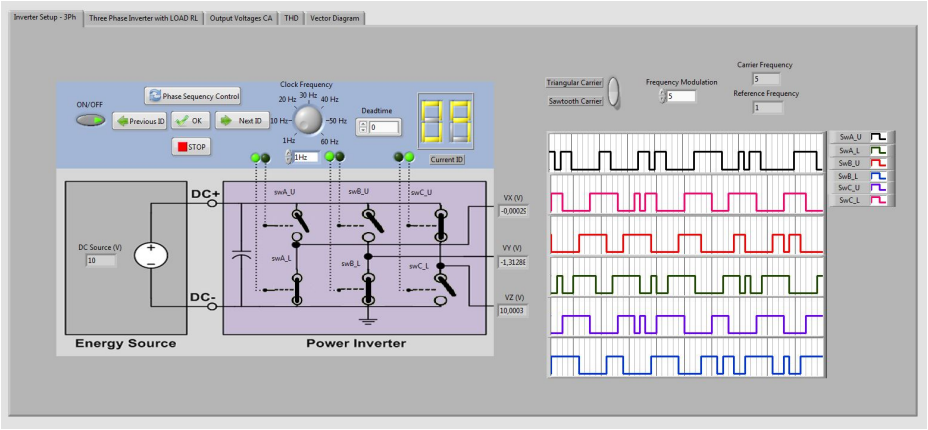

Figure 14. GUI Screen for ID = 08 with three phase full bridge VSI, THIPWM mode of operation.

3. Lab on A Chip

A Lab-on-a-Chip (LoC), whose concept that originated in biochemical analysis applications[12], is a device that integrates one or more *Laboratory Functions* into a single integrated circuit (commonly called a "chip"), to implement a practical approach of automation and implementation (On-a-Chip) of classroom experimentation lessons.

From a practical point of view, we can focus the implementation of a LoC within two aspects: (1) In technological aspects that comprise the telecommunication infrastructure embedded in a System-on-a-Chip (SoC)[11] that will provide secure and efficient remote access

to this device; and (2) In the methodological aspects, educational and pedagogical, that involve the construction of a practical program of teaching of a certain discipline that is potentially susceptible of being embedded in a SoC device for use in face-to-face and non-face-to-face teaching.

The two aspects are very important, and they are not exclusive, a practical and operational solution of a LoC necessarily involves these two aspects. However, in the present proposal, an approach is been adopted on the relevant and necessary aspects to build a practical of LoC solution from the educational point of view.

Then, and in full adherence to a novel trend[11], it is proposed that both the PEBPTP-VSI, in the form of a GUI structure of hands-on Authentic Learning support, that include the all pedagogical development previously described, and the unified controller previously developed in FPGA, are embedded to constitute a Lab-on-a-Chip (LoC) structure for laboratory experimentation. This embedded structure will allow access to the laboratory hands-on program via a web service that uses a fully programmable logic device (PLD) that incorporates an integrated structure known as SoC embedded device as shown in Figure 15.

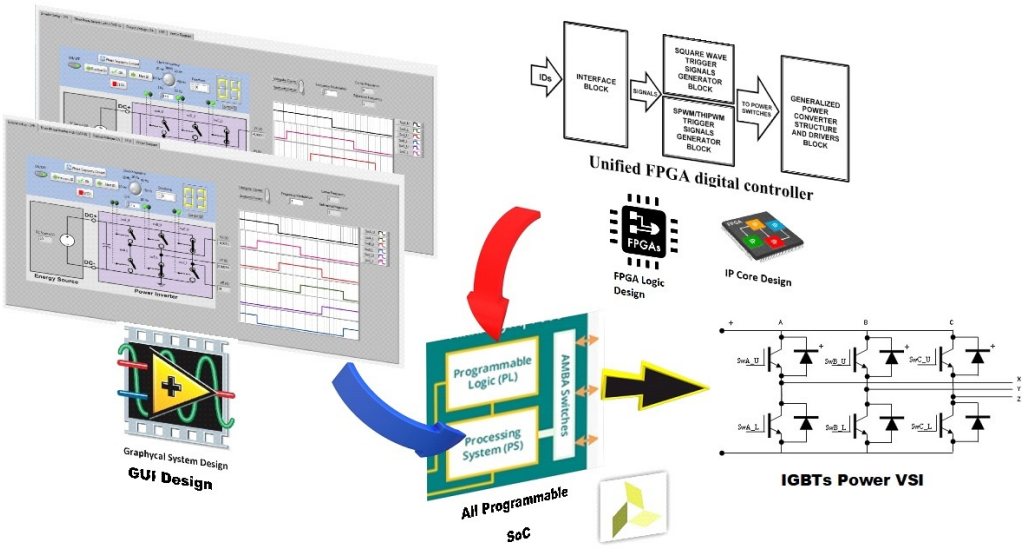

Figure 15. All Programmable SoC – LoC Design.

4. Conclusions

It is more than propagated in pedagogical environments that learning is facilitated when the student participates in the process. The mere transmission of information without adequate contextualization or even reception by the student does not affect an effective process of teaching and learning.

The training of innovative, autonomous and enterprising Engineers is always sought after by Engineering educators and there is a growing demand for methodologies that had better qualify Engineering students at Universities. The Active Methodologies, converging with the diverse possibilities of resources of the DICTs, with the adequate contextualization of the specific resources of each area, contribute increasingly for the student to be protagonist of their knowledge.

The above proposals and experiences involve the mastery not only of curricular and technological knowledge, inherent to the training of an Engineer, but of mainly, the pedagogical technological knowledge and correct use of DICTs. At this point, in particular, is founded our contribution within the context of Engineering Teaching, to advance in the improvement or perhaps in the modification of the "classroom" of Engineering courses, which today go beyond the physical space of the University.

All the aspects of construction of a PEBPTP-VSI, presented in this work, were developed and tested in laboratory. The application of this new pedagogical strategy is under way. It is intended gradually to implant this culture within the UFMA's Electrical Engineering Course, expanding this practice to other disciplines.

Access to the remote lab, like a LoC, is possible via the Internet, since the embedded system runs a Web Server that exposes online the projected GUI enabling Laboratory Functions to be executed remotely. With regard to future development, we are migrating the system to a platform Xilinx Zynq SoC, which have improved capabilities, which would enable updating the PEBPTP-VSI during runtime.

Acknowledgment

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